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| Serial No: |
| **Sessional II** |
| **Total Time: 1 Hour** |
| **Total Marks: 60** |
| \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_  Signature of Invigilator |

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| **EE-227 Digital**  **Logic Design** |
| Monday 2nd April, 2018 |
| **Course Instructor** |
| Dr. Mewhish Hassan, Mehreen Alam,  Rabia Bannu |

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## DO NOT OPEN THE QUESTION BOOK OR START UNTIL INSTRUCTED.

**Instructions:**

1. Attempt on question paper. Attempt all of them. Read the question carefully, understand the question, and then attempt it.
2. No additional sheet will be provided for rough work. Use and mark the back of the last page for rough work.
3. If you need more space write on the back side of the paper and clearly mark question and part number etc.
4. After asked to commence the exam, please verify that you have **Seven (7)** different printed pages including this **Title page** and **Rough work page** at the end. There are total of **4 questions**.
5. **Calculator is NOT allowed**.
6. Use permanent ink pens only. Any part done using soft pencil will not be marked and cannot be claimed for rechecking.
7. **For each question show your complete method in solution to get full credit**.

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|  | Q-1 | Q-2 | Q-3 | Q-4 | **Total** |
| **Total**  **Marks** | **10** | **10** | **27** | **13** | **60** |
| **Marks Obtained** |  |  |  |  |  |

**Vetted By: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ Vetter Signature: \_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

Question No.1 [ 10 pts ]

Design a NAND logic circuit that implements the function: F(A,B,C,D) = ∑ (0,1,2,3,6,10,11,14)

Question No.2 [ 10 pts ]

Implement the following function using don’t care conditions using no more than two NOR gates.

F(A,B,C,D) = ∑ (2,4,10,12,14)

d(A,B,C,D) = ∑ (0,1,5,8)

**Question No.3 [ 2+5+5+5+5+5 = 27 pts ]**

Implement the function, F (A,B,C,D) = ∏ (2,6,11) using:

1. One 16 x 1 multiplexer only.
2. 8 x 1 multiplexers and any external gates only.
3. 4 x 1 multiplexers and any external gates only.
4. One 4 x 16 decoder only.
5. 3 x 8 decoders and any external gates only.
6. 2 x 4 decoders and any external gates only.

**Question No.4 [ 13pts ]**

Fill in the following table for an eight-bit priority encoder with the following priorities:

**D1 > D0 > D7 > D3 > D6 > D2 > D5 > D6 > D4**

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| **Inputs** | | | | | | | | **Outputs** | | | |
| **D0** | **D1** | **D2** | **D3** | **D4** | **D5** | **D6** | **D7** |  | **x** | **y** | **z** |
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**Rough Work**